

FIG.1A

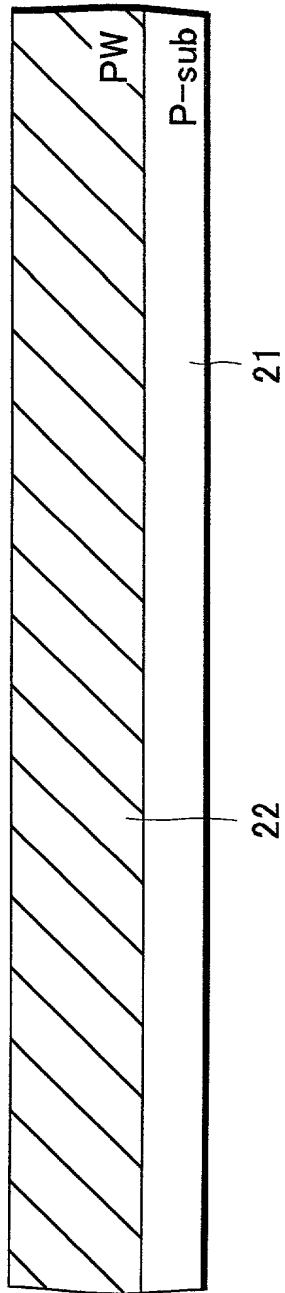


FIG.1B

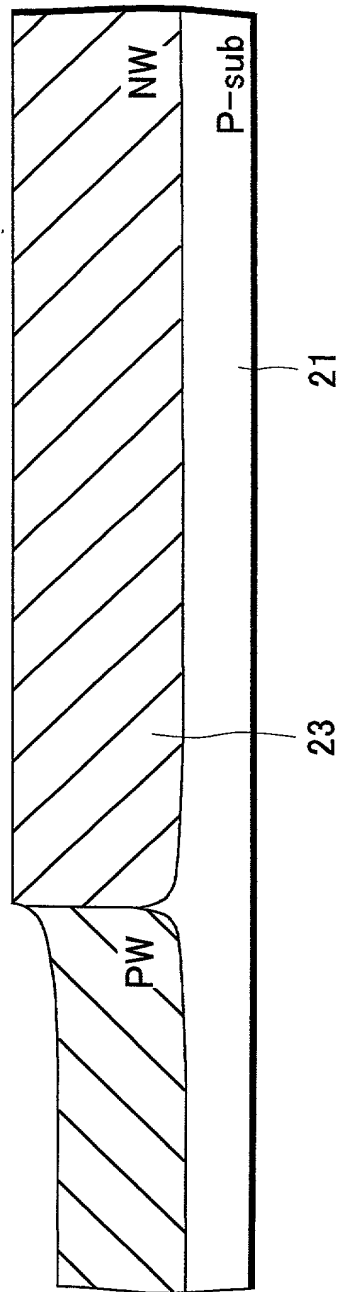


FIG.2A

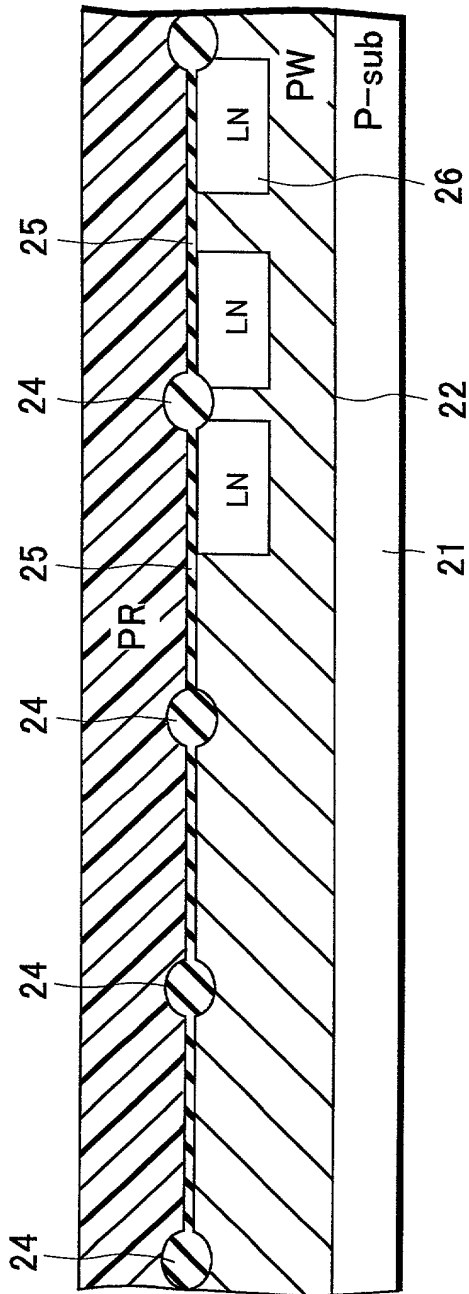


FIG.2B

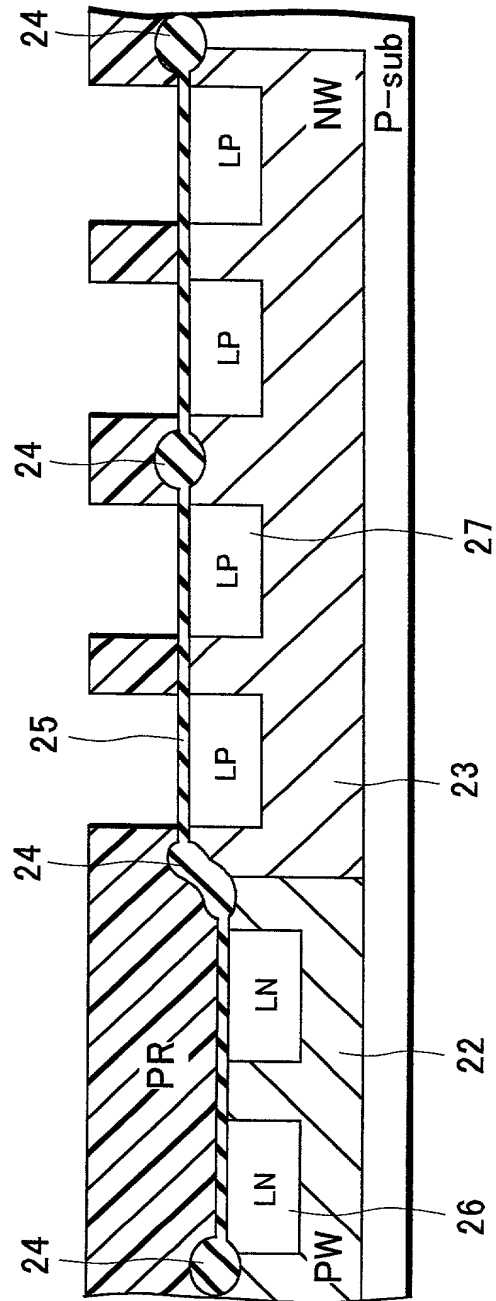


FIG.3A

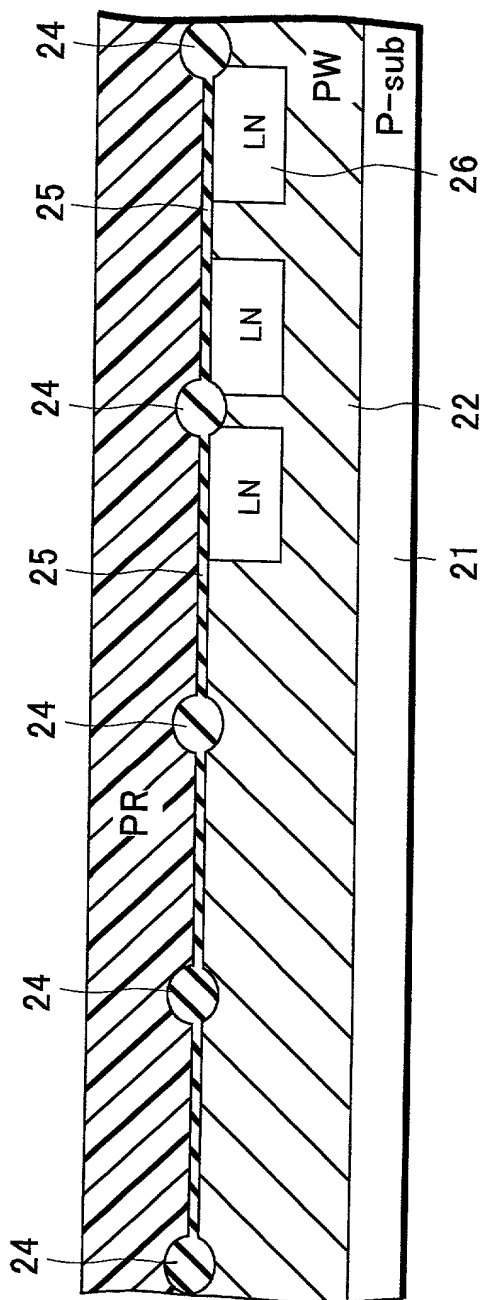


FIG.3B

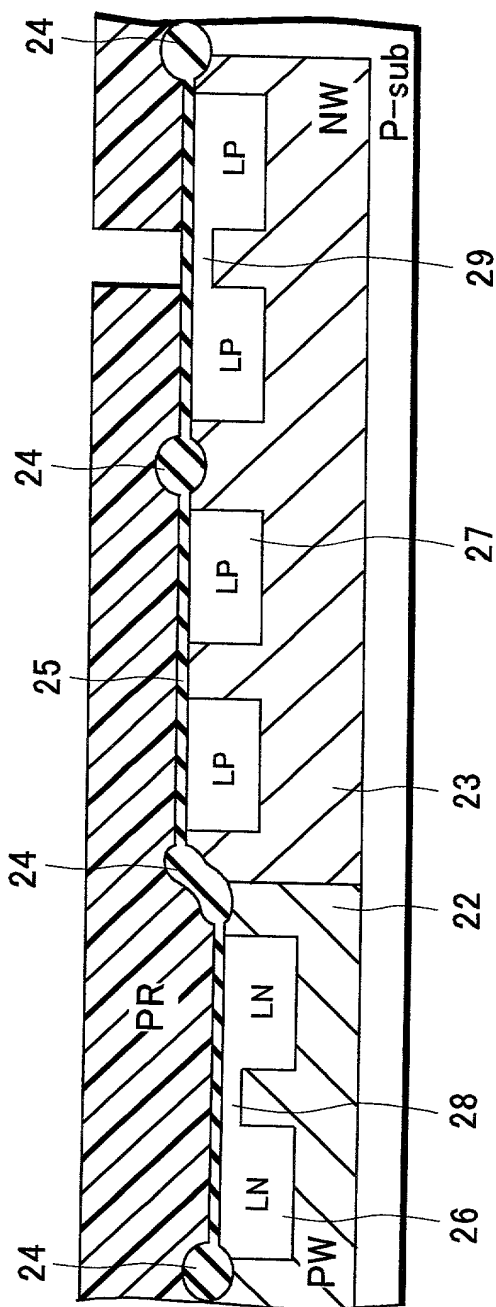


FIG.4A

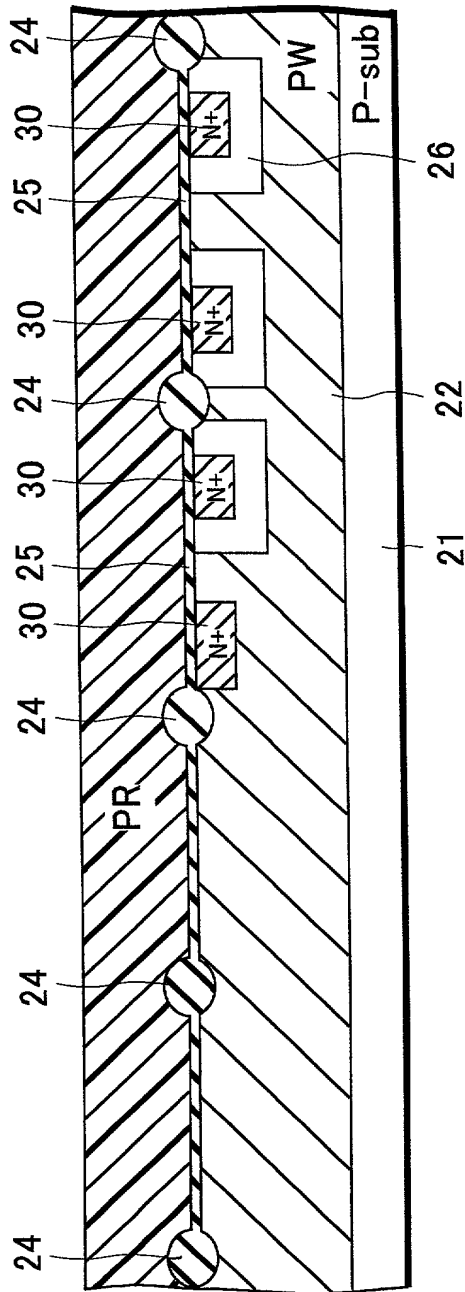


FIG.4B

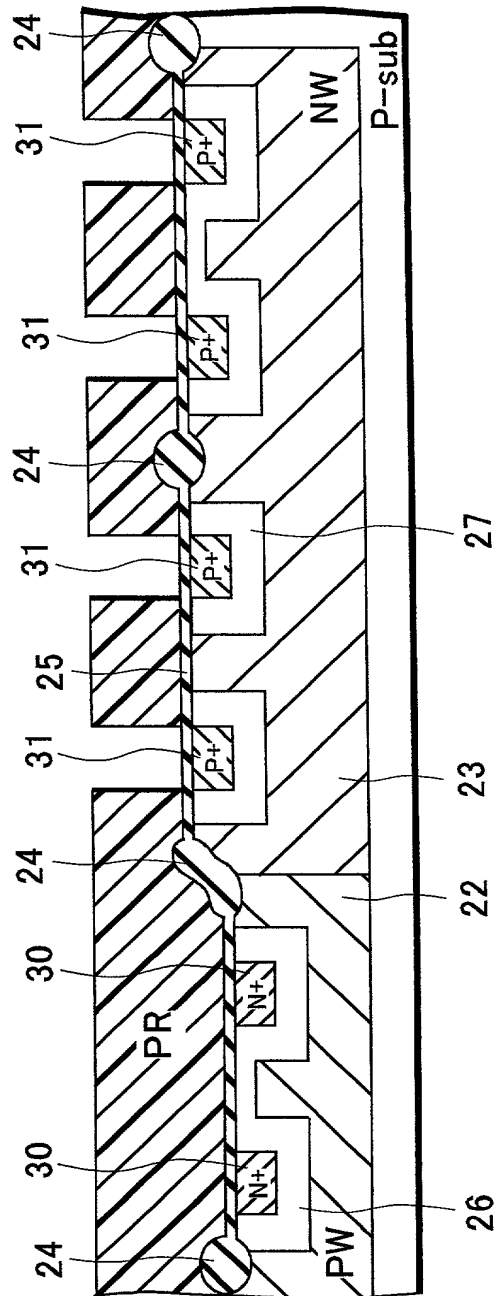


FIG.5A

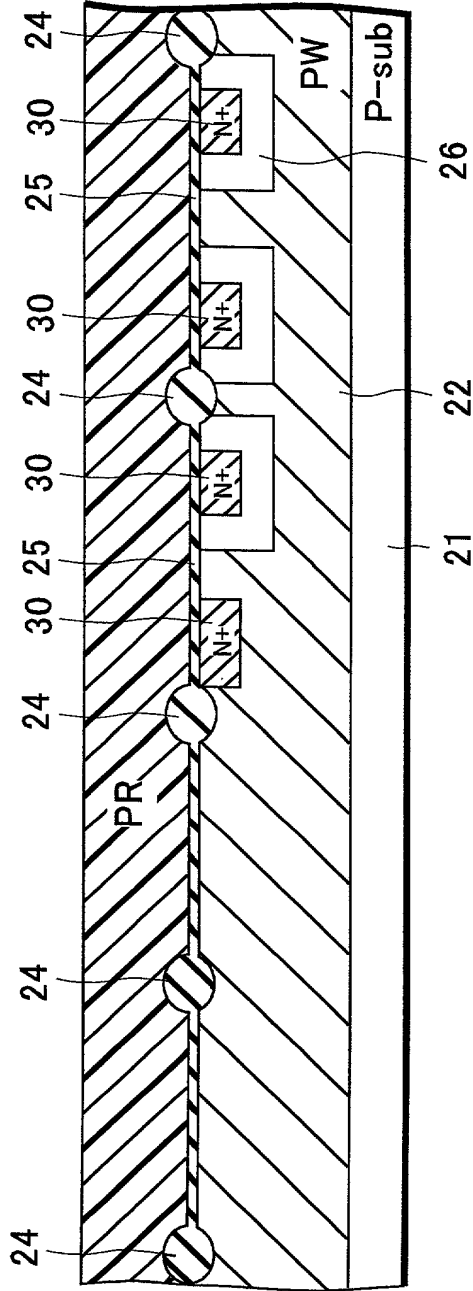


FIG.5B

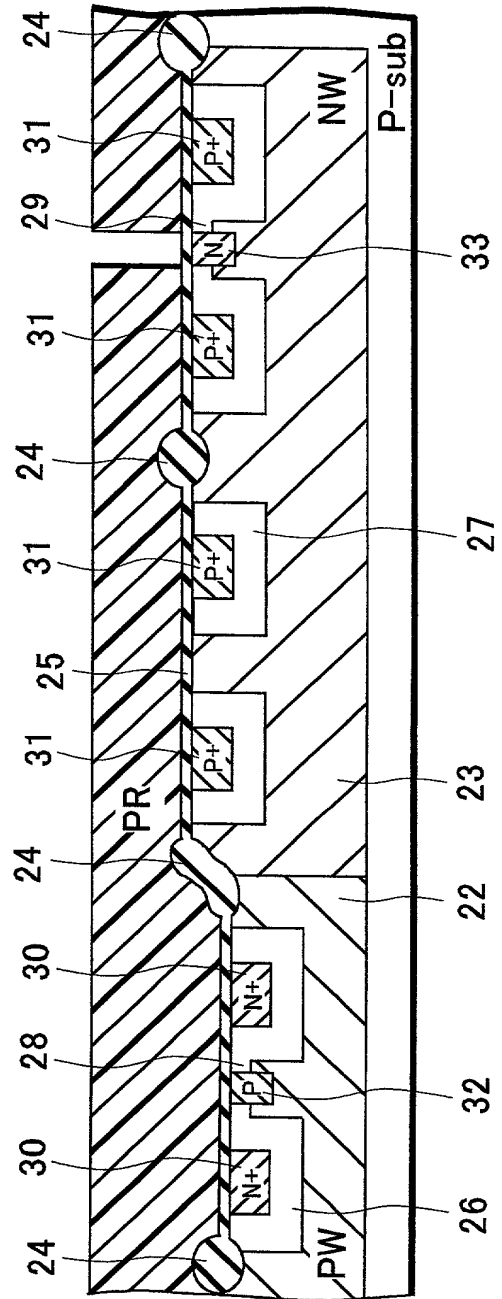


FIG.6A

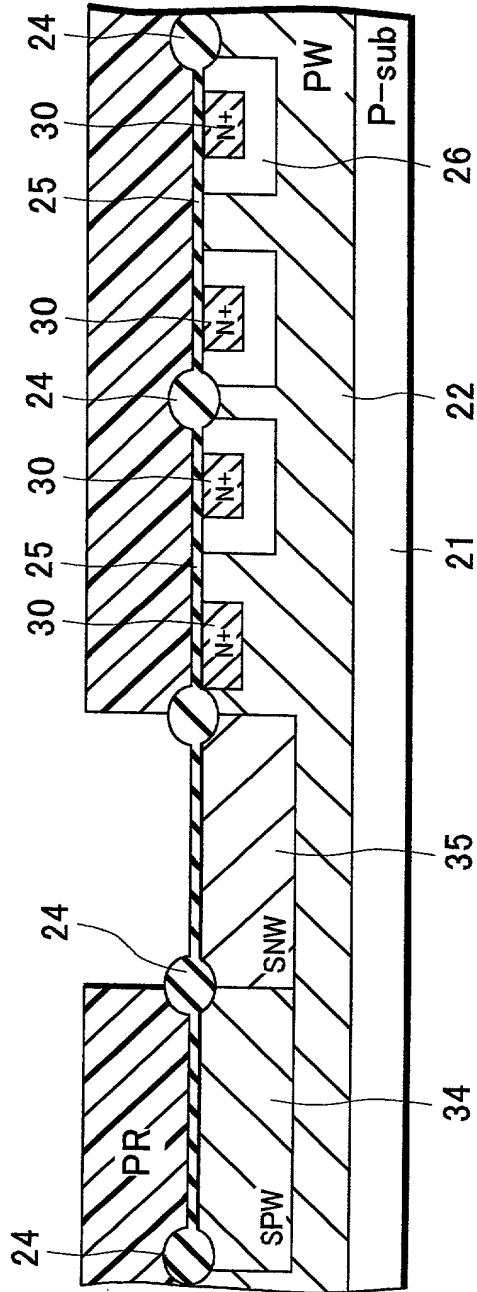


FIG.6B

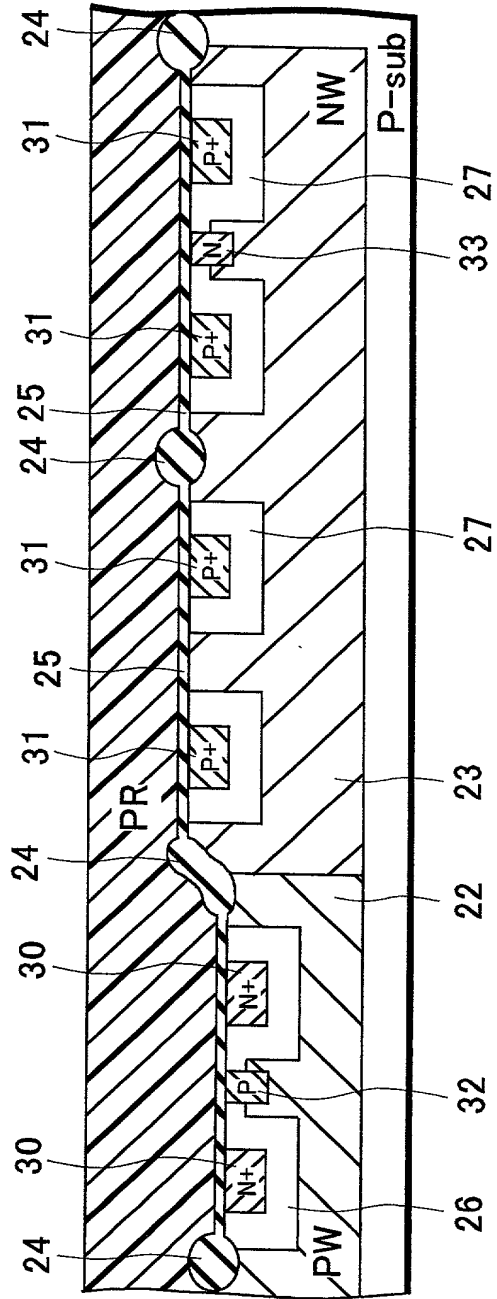


FIG. 7A

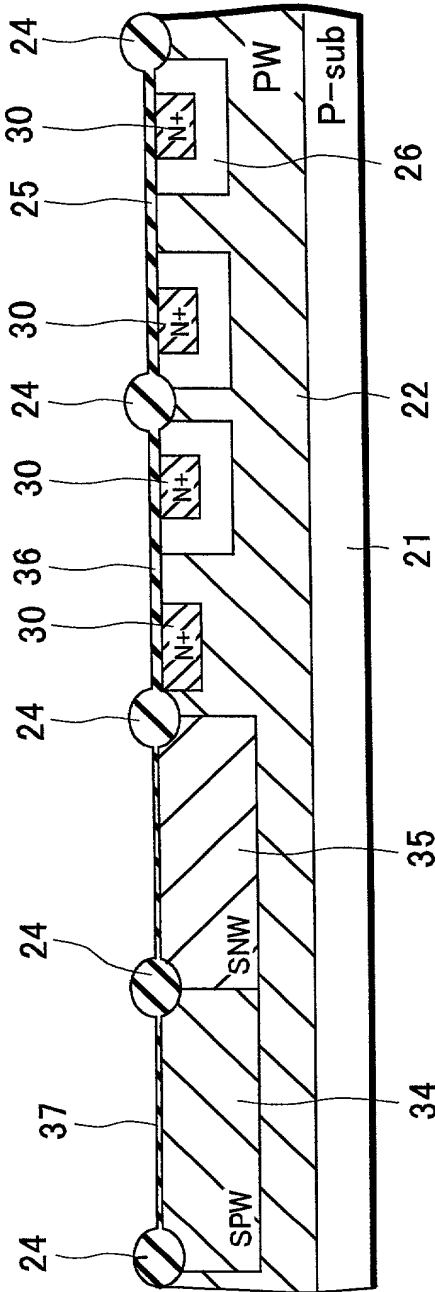


FIG. 7B

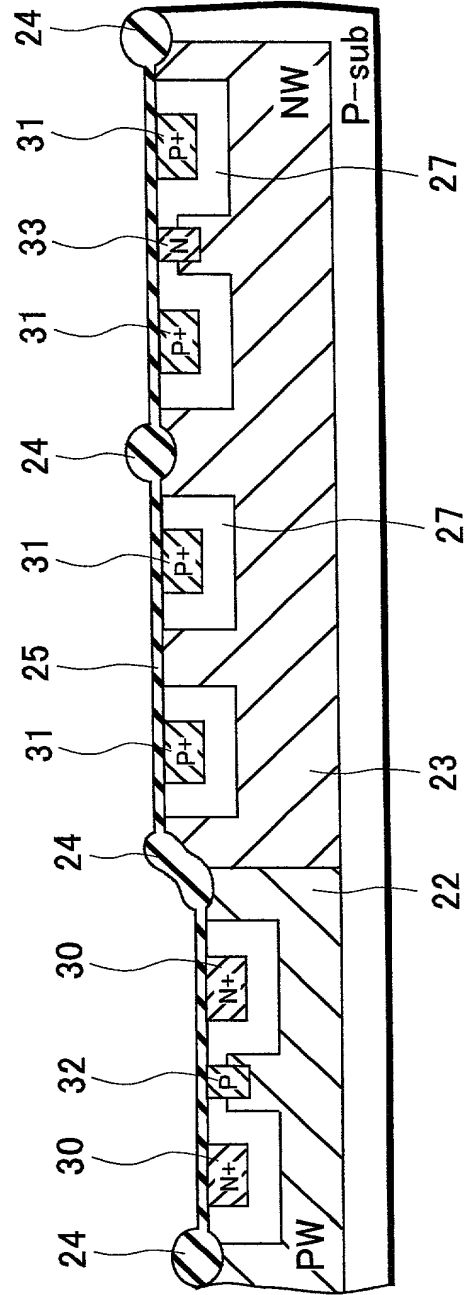


FIG.8A

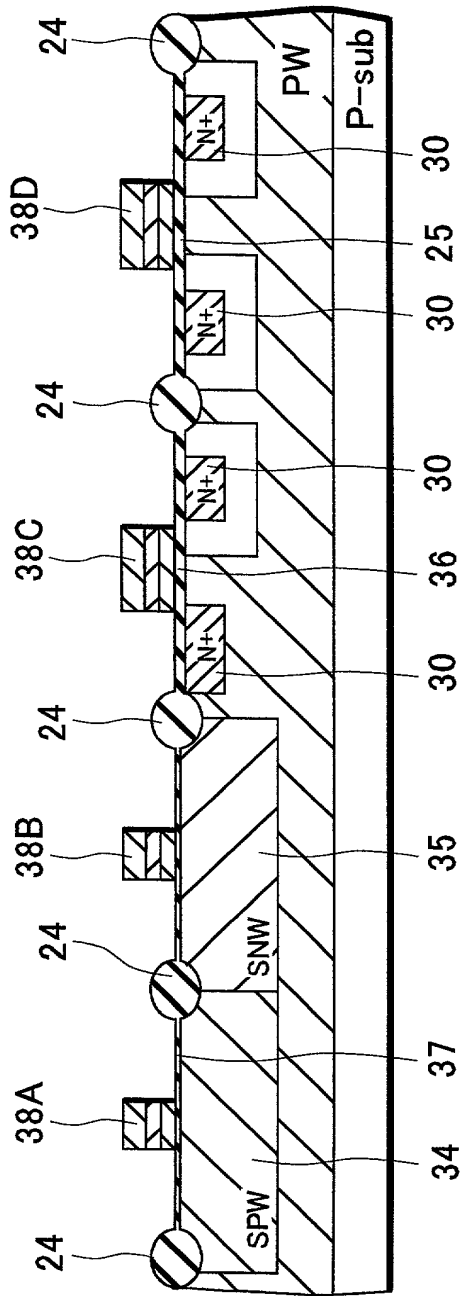
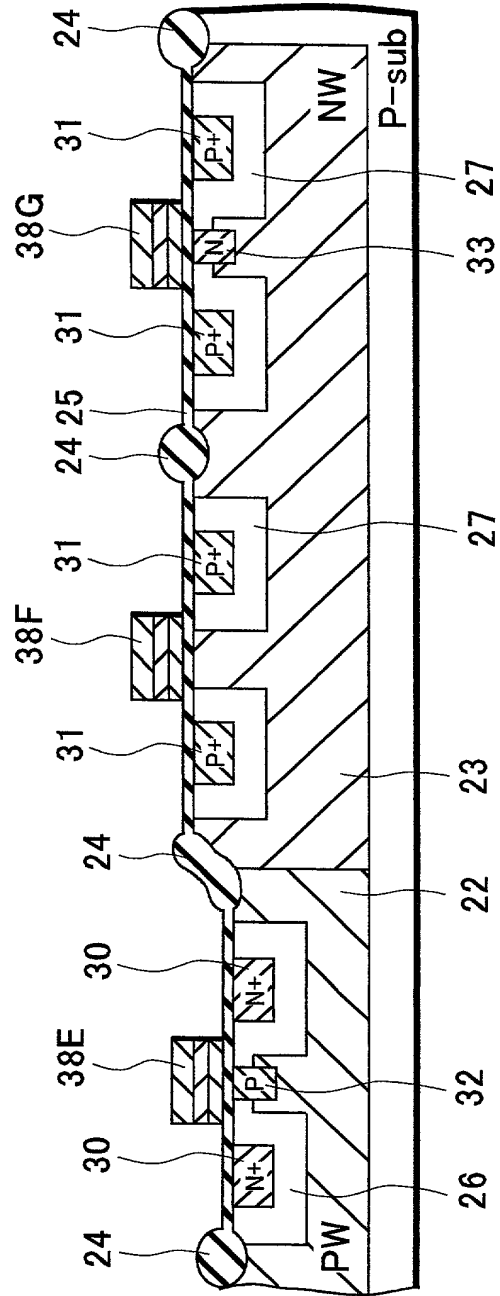


FIG.8B





This cross-sectional view shows a semiconductor device with a substrate labeled 'P-sub'. The device features several regions: 'SPW' (Semiconductor Patterned Wafer) at the bottom left, followed by 'N-' regions, 'N+' regions, and 'PR' (Passivation Layer) regions. The top surface is covered by a 'PW' (Passivation Wafer) layer. The device is divided into sections labeled 24, 38A, 38B, 38C, and 38D. The right side of the device is labeled 'P-sub' and '30'.

This cross-sectional view shows a semiconductor device with a P-substrate (27). The device features a series of gate structures (23) on top of a channel region (22). The gate structures are labeled with various regions: PW (26), N+ (30), P+ (32), and NW (31). The gate structures are separated by spacers (24). The device is shown in a cross-section along a line A-A'.

FIG.10A

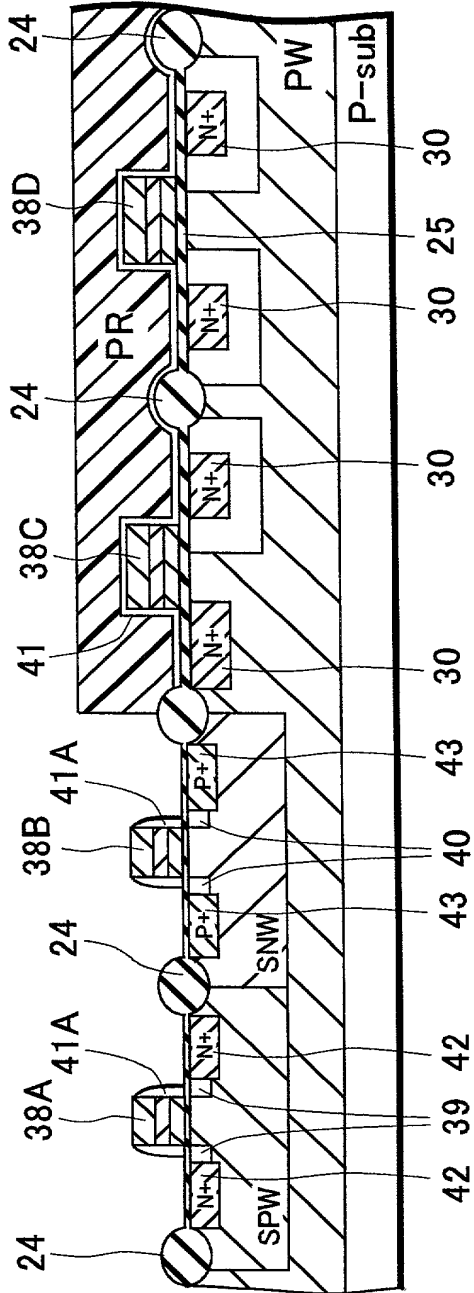


FIG.10B

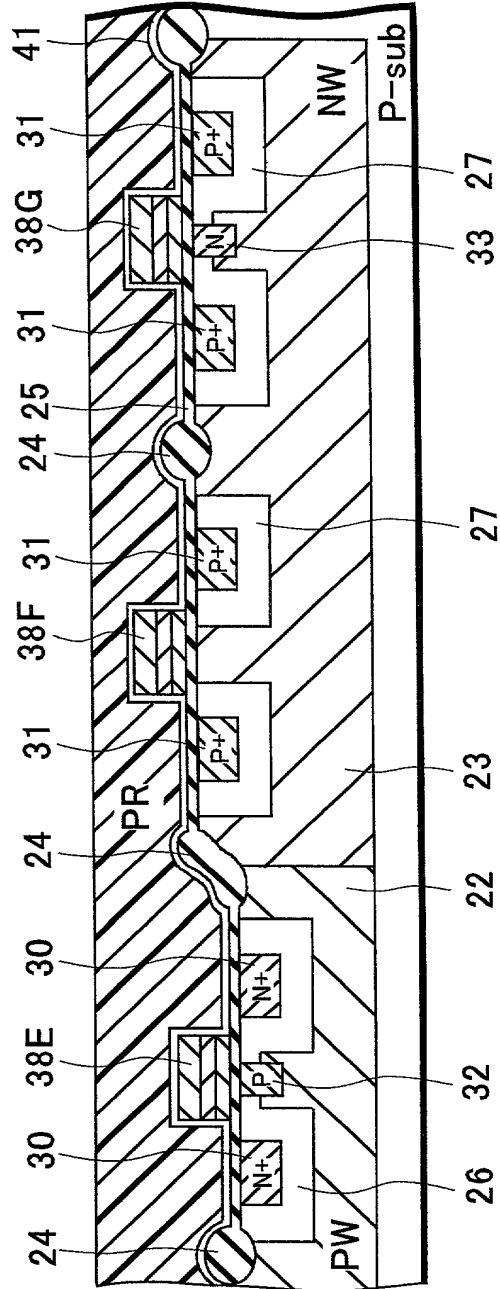


FIG.11A

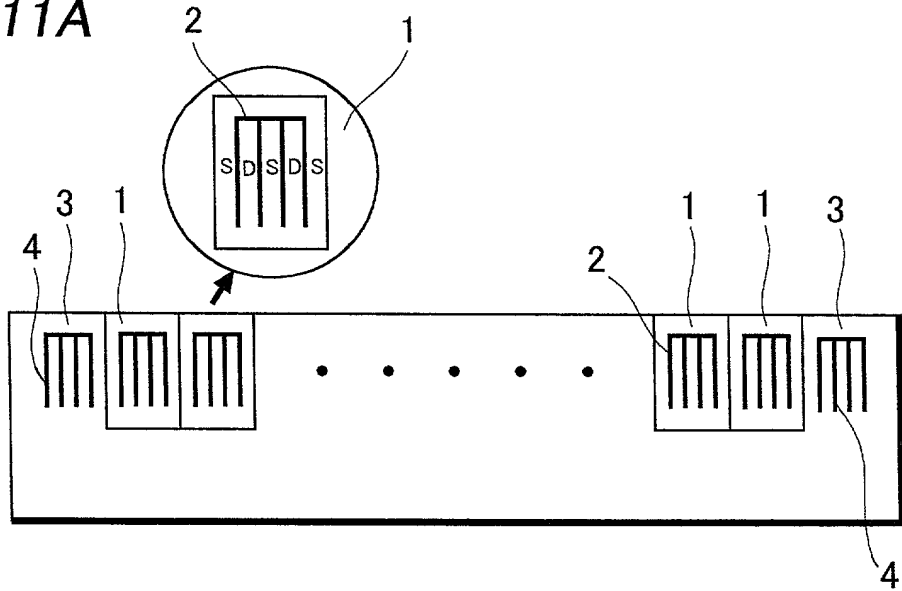


FIG.11B

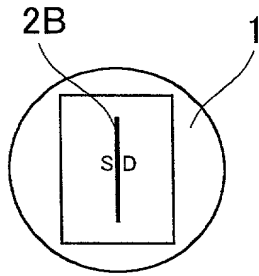


FIG.11C

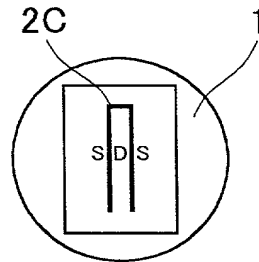
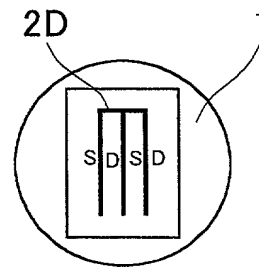


FIG.11D



[illegible]